

Notice of Allowability

Application No.

10/726,964

Examiner

Tuan T. Lam

Applicant(s)

JURGILEWICZ ET AL.

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 4/5/2005.
2. ☒ The allowed claim(s) is/are 1-10 and 18-32.
3. ☒ The drawings filed on 05 April 2005 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413), Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____ |


TUAN T. LAM
PRIMARY EXAMINER

Art Unit: 2816

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Abstract:

Line 8, after "transistor.", --One embodiment includes the low voltage pull-down circuit in a power supervision circuit for systems that operate with, for example, low power conditions. The open-drain node is utilized as power-on-reset node that provides a low logic signal to a system when the power being supplied to the system is below a predetermined voltage threshold.--

Delete the entirety of the second paragraph.

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance: the amendment filed 4/5/2005 has overcome the prior art of record and the technical deficiencies. The prior art of record fails to teach or fairly suggest a control node (V_{up} of figure 2), wherein said output node is pulled up to a logic high voltage when a logic high voltage is applied to said control node as called for in claim 1, a third sub circuit comprising a fourth and fifth NMOS transistors coupled to the input node and the ground terminal as called for in claim 18, a pull down transistor coupled to said first sub circuit, wherein said output node is pulled up when a voltage high is applied to the gate terminal of said pull down transistor (transistor 242 of figure 2), an intermediate node, a resistor, a first PMOS switch, wherein the source terminal of said first PMOS switch is coupled to said input node, the gate terminal of said first PMOS switch is

Art Unit: 2816

coupled to said intermediate node, and the drain terminal of said first PMOS switch is coupled to the source terminal of said first NMOS transistor as called for in claim 26, a current mirror coupled to said first sub circuit for controlling the amount of current at said output node as called for in claim 27, an electrostatic discharge cell coupled to said first and second sub circuits as called for in claim 28, a second sub circuit comprises third and fourth NMOS transistors, wherein the threshold voltage of the third and fourth transistors is greater the threshold voltage of the first and second NMOS transistors, the threshold voltage of the fifth transistor is greater than the threshold voltage of the third and fourth transistors as called for in claim 30, a plurality of inputs, a plurality of power supervision circuits, wherein each one of said plurality of power supervision circuits is coupled to one of said plurality of inputs, each one of said plurality of power supervision circuits is coupled to said output, a logic low is placed on said output when the voltage of at least one of said plurality input is below at least one predetermined voltage level as called for in claims 31 and 32. Therefore, claims 1-10 and 18-32 are presently allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

Art Unit: 2816

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan T. Lam
Primary Examiner
Art Unit 2816

05/03/2005

2/7

*Approved
Plan
5/3/05*

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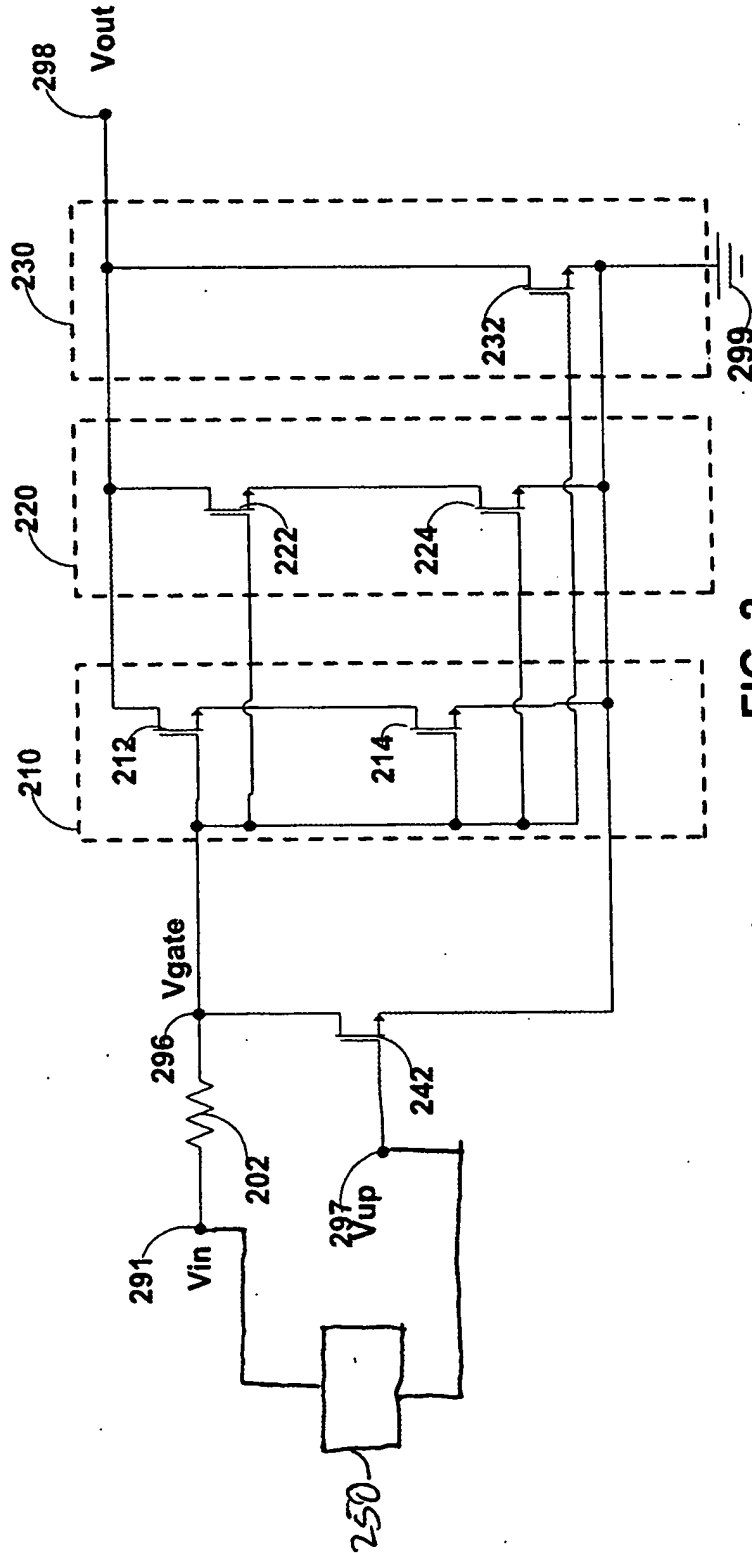


FIG. 2

2/7



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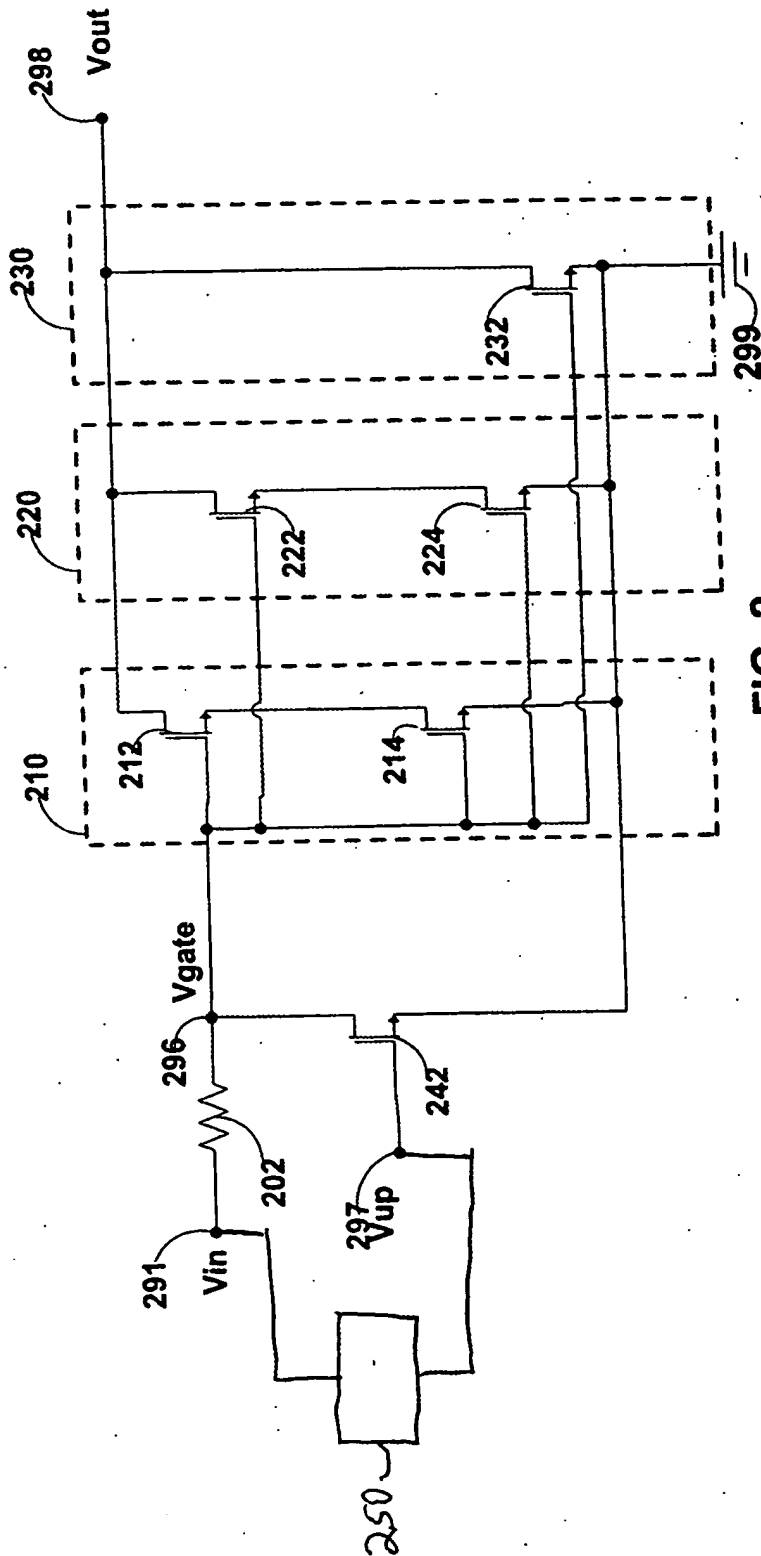


FIG. 2